

Amendments to the Claims:

1. (currently amended) A computer based system employing a customizable Simulation Model of an ATM/SONET Framer, for system level verification and performance characterization, comprising:

means for developing an accurate customizable behavioral model that offer sufficient parameters which can be programmed to represent Framers from different vendors;

a Receiver system; means for providing two independently configurable components, a Receiver and a Transmitter which provide testing with said framers from multiple vendors by changing programmable parameters of said model

a Transmitter system wherein said Receiver system and said Transmitter system are independently configurable and each includes a UTOPIA interface programmable to provide different protocols;

a first group of buffers operatively coupled to the UTOPIA interface;

SONET Framer Processes including a format translator; and

a second group of buffers operatively coupled to the SONET Framer Processes.

2. (Previously presented) The system of claim 1 wherein said ATM/SONET Framer provides at least one Receive and at least one Transmit interfaces to the network at a SONET line rate of 155.52 Mbps(OC-3), 622.08 Mbps(OC-12) and 2488.32 Mbps(OC-48).

3. (Currently amended) The system of claim 13 wherein said ATM clock domain and said SONET clock domain interfaces operate on different clock frequencies and represent two distinct clock domains. ~~domains;~~
~~and~~

~~the data interchange between the two said clock domains is achieved by means of FIFO buffer elements and associated control and status signals.~~

4-5. (Canceled)

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6. (Currently amended) The system of claim ~~[[4]]~~ 1 which in addition, offers programmability, rich feature set, and two independently configurable models, one each for said transmit side and said receive side,
and

offers said programmability features of:

- . SONET line rates (OC-Nc: N=1..48; OC-1=51.48 Mbps)
- . Percentage of data bytes vs. overhead bytes
per row
- . Delays associated with clock domain
synchronization
- . FIFO depth and threshold (in terms of number of
cells)
- . Byte or word count threshold within a cell
associated with FIFO status update
- . UTOPIA Level-2/3
- . Built-in performance checking

7-12. (Canceled)

13. (New) The computer base system of claim 1 wherein the first group of buffers and the Utopia interface are positioned in an ATM clock domain and the SONET Framers Processes and the second group of buffers are placed in a SONET clock domain.

14. (New) A computer base method for system level verification and performance characterization comprising:

providing a customized behavioral model of an ATM/SONET Framer which includes independently configurable Receiver system and Transmitter system;

providing software for coacting with said behavioral model, said software including sufficient programmable parameters for representing Framers from different vendors; and

activating selected ones of said programmable parameters which cause the model to behave as a framer from a particular framer manufacturer.

15. (New) The method of claim 14 further including providing additional parameters, that causes the model to operate at different line rates.

16. (New) The method of claim 15 further including activating selected ones of the additional parameters to cause the model to operate at one of a plurality of line rates.

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17. (New) The computer based system of claim 1 wherein the format translator converts ATM cells to SONET packets and visa versa.

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